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10/598,934	09/15/2006	Seiji Nakahata	039.0075	2278

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EXAMINER	
AHMED, SELIM U	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,934	NAKAHATA ET AL.	
	Examiner	Art Unit	
	SELIM AHMED	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response filed on 03/19/2009 is acknowledged. Applicants have amended claims 1-10 and 12-21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Objections

2. Claims 12-21 are objected to because of the following informalities:

Claim 12 recites, "...a step of separating from said starting substrate Group III nitride semiconductor crystals..." The claim fails to point out what is being separated from said starting substrate. The claim should read, "...a step of separating said starting substrate from Group III nitride semiconductor crystals..." similar to claim 1.

The dependent claims 13-21 inherit the deficiencies.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 recites the limitations "said Group III nitride semiconductor crystal substrate", "said Group III nitride semiconductor crystal substrates", "said Group III nitride semiconductor crystal layers" in lines 6, 8, and 9 respectively. There are insufficient antecedent basis for these limitations in the claim.

The dependent claims 13-21 inherit the deficiencies.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-10, 12-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong et al (US 6,617,261; Wong hereinafter).

With regard to claim 1, Wong discloses a Group III nitride semiconductor crystal manufacturing method (e.g. Figs. 9-14), comprising: a step of growing at

least two (Fig. 12, elements 218) Group III nitride semiconductor crystals (col. 8, line 17) on a starting substrate 200; and a step of separating (e.g. Fig. 14; cols. 8/9, lines 54-9) said Group III nitride semiconductor crystal 218 from said starting substrate 200; characterized in that said Group III nitride semiconductor crystals 218 each are 10 um or more but 600 um or less in thickness (col. 7, lines 45-50; col. 8, line 18), and each are 0.2 mm or more but 50 mm or less in width (cols. 7/8, lines 60-7).

With regard to claim 2, e.g. Fig. 12 of Wong discloses the Group III nitride semiconductor crystal 218 manufacturing method recited in claim 1, characterized in that the principal faces (top surfaces of all of the 218) of said Group III nitride semiconductor crystals 21 together are smaller in area than the principal face (top surface of 200) of said starting substrate 200 (since there are 220 trenches, principal faces of 218 together are smaller in area than principal face of the starting substrate 200).

With regard to claim 3, e.g. Figs. 10-12 of the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that said step of growing at least two said Group III nitride semiconductor crystals 218 includes: a step of forming on said starting substrate 200 a mask layer 206 (or 210) having at least two windows 212; and a step of growing each said Group III nitride semiconductor crystal 218 at least on an open surface 212 of said

starting substrate 200 below a respective one of said windows 212 in said mask layer 206 (or 210).

With regard to claim 4, e.g. Fig. 10 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 3, characterized in that said windows 212 each are formed from a group composed of at least two micro-apertures (212 are formed by patterning through micro-apertures).

With regard to claim 5, e.g. Fig. 10 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that said step of growing at least two said Group III nitride semiconductor crystal 218 includes: a step of disposing at least two seed crystals 202 on said starting substrate 200; and a step of growing said Group III nitride semiconductor crystals 218 with said seed crystals as their respective nuclei (col.8, lines 58-60).

With regard to claim 6, e.g. Fig. 14, element 234 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that whichever of an etching, lasing 234, or cleaving method is used in said step of separating from said starting substrate said Group III nitride semiconductor crystals 218.

With regard to claim 7, e.g. col.8, line 11 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that the conformation of said Group III nitride semiconductor crystals is hexagonal-platelike, rectangular-platelike, or triangular-platelike.

With regard to claim 8, e.g. col.4, line 55 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that said Group III nitride semiconductor crystals 218 are grown at a rate of at least 10 um/hr but not more than 300 um/hr.

With regard to claim 9, e.g. cols. 4/5, lines 67-1 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 1, characterized in that said Group III nitride semiconductor crystals have an impurity concentration that is not more than 5 x 1019 cm-3.

In light of claim objection and 112, 2nd rejection above, with regard to claim 12, Wong discloses a method of manufacturing a Group III nitride semiconductor device (e.g. Figs. 9-14), comprising: a step of growing at least two Group III nitride semiconductor crystal substrates (Fig. 12, elements 204; col. 7, line 48) of semiconductor-device-scale dimension (a discrete value of the device scale dimension is not required by claim, so any dimension that is right for semiconductor device can be used i.e. Wong's dimension of 204 being 2 um that

can be said as semiconductor device scale dimension) on a starting substrate 200; a step of growing at least one Group III nitride semiconductor crystal layer 216 on each said Group III nitride semiconductor crystal substrate 204; and a step of separating (e.g. Fig. 14; cols. 8/9, lines 54-9) said starting substrate 200 from Group III nitride semiconductor crystals (204 and 216) that are constituted by said Group III nitride semiconductor crystal substrates 204 and said Group III nitride semiconductor crystal layers 216; characterized in that said Group III nitride semiconductor crystals (204 and 216) each are 10 um or more but 600 um or less in thickness (col. 7, lines 45-50; col. 8, line 18), and each are 0.2 mm or more but 50 mm or less in width (cols. 7/8, lines 60-7).

With regard to claim 13, e.g. Fig. 12 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that the principal faces (top surfaces of the 204/216) of said Group III nitride semiconductor crystals together are smaller in area than the principal face (top surface of 200) of said starting substrate 200 (since there are trenches 220, principal faces of 204/216 together are smaller in area than principal face of the starting substrate 200).

With regard to claim 14, e.g. Figs. 10-12 of the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that said step of growing at least two said Group III nitride semiconductor crystals (204/216) includes: a step of forming on said starting substrate 200 a mask layer 206 (or 210) having at least two windows 212; and a step of growing each said Group III nitride semiconductor crystal (204/216) at least on an open surface 212 of said starting substrate 200 below a respective one of said windows 212 in said mask layer 206 (or 210).

With regard to claim 15, e.g. Fig. 10 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 14, characterized in that said windows 212 each are formed from a group composed of at least two micro-apertures (212 are formed by patterning through micro-apertures).

With regard to claim 16, e.g. Fig. 10 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that said step of growing at least two said Group III nitride semiconductor crystal (204/216) includes: a step of disposing at least two seed crystals 202 on said starting substrate 200; and a step of growing said Group III nitride semiconductor crystals (204/216) with said seed crystals as their respective nuclei (col.8, lines 58-60).

With regard to claim 17, e.g. Fig. 14, element 234 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that whichever of an etching, lasing 234, or cleaving method is used in said step of separating from said starting substrate said Group III nitride semiconductor crystal (204/216) constituted by said Group III nitride semiconductor crystal substrate 204 and said Group III nitride semiconductor crystal layers 216.

With regard to claim 18, e.g. col.8, line 11 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that the conformation of said Group III nitride semiconductor crystals is hexagonal-platelike, rectangular-platelike, or triangular-platelike.

With regard to claim 19, e.g. col.4, line 55 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that said Group III nitride semiconductor crystals 218 are grown at a rate of at least 10 um/hr but not more than 300 um/hr.

With regard to claim 20, e.g. cols. 4/5, lines 67-1 of Wong discloses the Group III nitride semiconductor crystal manufacturing method recited in claim 12, characterized in that said Group III nitride semiconductor crystals (204/216) have

an impurity concentration that is not more than 5 x 1019 cm-3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Tsuda et al (US 2003/0136957; Tsuda hereinafter).

With regard to claim 10 or 21, Wong discloses all of the limitations of claim 1 or 12 respectively with the exception of the Group III nitride semiconductor crystal manufacturing method, characterized in that an off angle between the principal face of said Group III nitride semiconductor crystals and whichever of their (0001) face, (1200) face, (1120) face, (1101) face, (1102) face, (1121) face, or (1122) face is 0° or more but not more than 4°. However, e.g. in para[0027] of Tsuda discloses an off angle between the principal face of said Group III nitride semiconductor crystal and whichever of its (0001) face, (12OO) face, (1120) face, (1101) face, (1102) face, (1121) face, or (1122) face is 0° or more but not more than 4° . In para[0027] of Tsuda discloses, "If a substrate has an off-angle within 2 degree from those surface orientations, the semiconductor crystal layer

grown thereon has a good surface morphology". It would have been obvious to one having ordinary skill in the art at the time of the invention to have Tsuda's characterization of off- angle within Wong's device for predictable results.

Response to Arguments

6. Applicant's arguments with respect to claims 1-10, 12-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826